DS1000 Board CPLD Design Specification

Revision 0.8

.

1 Revision History

Version	Date	Author	Approver	Description
0.1	2021/04/15			First Draft.
0.2	2021/05/24			
0.3	2021/06/08			
0.4	2021/07/01			
0.5	2021/07/06			
0.6	2021/10/26			1.Change Watch dog register 2.Change PSU LED register 0xA142
0.7	2021/11/08			1.Add register 0xA181 Switch power control register
0.8	2021/12/03			1.Change register 0xA147 2.Add register 0xA1F3

2 Table of Contents

1 Revision History 2

2 Table of Contents 3

3 Table of Figures 5

4 Table of Tables 6

5 Introduction 8
5.1 Audience 8
5.2 Purpose 8
5.3 Glossary 8

6 Functional Description 9
6.1 Functionality 9
6.1.1 Feature List 9
6.1.2 Power Control 9
6.1.2.1 System Power Sequence 9
6.1.2.2 Switch Power sequence 10
6.1.3 I2C Slave Interface 11
6.1.4 FAN Control 12
6.1.4.1 FAN speed control 12
6.1.4.2 FAN WDT 13
6.1.5 Reset Topology 13
6.1.6 Interrupts 14
6.1.7 BIOS Boot Control 15
6.1.8 Thermal Shutdown Control 16
6.1.9 LED Control 16

7 Software Interface 17
7.1 Register mapping 17
7.2 Registers in CPLD_B 19
7.2.1 Register 0xA100: CPLD_B Version Register 19
7.2.2 Register 0xA101: CPLD_B Software Scratch Register 19
7.2.3 Register 0xA102: CPLD_B MONTH Register 19
7.2.4 Register 0xA103: CPLD_B DATA Register 19
7.2.5 Register 0xA104: CPLD Bit Source Register 19
7.2.6 Register 0xA105: CPU Reset Source Register 19
7.2.7 Register 0xA106: Reset Control Register 20
7.2.8 Register 0xA107: BCM56277 Reset Control Register 20
7.2.9 Register 0xA108: CB_RST_N Mask Register 20
7.2.10 Register 0xA109: PHY1 Reset Control Register 20
7.2.11 Register 0xA10A: PHY2 Reset Control Register 21
7.2.12 Register 0xA110: PHY3 Reset Control Register 21
7.2.13 Register 0xA111: COMe Power Control Register 21
7.2.14 Register 0xA112: COMe Reset Control Register 21
7.2.15 Register 0xA113: COMe Status Register 21
7.2.16 Register 0xA114: COMe BIOS Disable Control Register 22
7.2.17 Register 0xA115: COMe_BIOS_DIS_CTRL Register 22
7.2.18 Register 0xA116: COMe Power Button Control Register 22
7.2.19 Register 0xA117: RTC_CLEAR_CTRL Register 22
7.2.20 Register 0xA118: Power Cycle Control Register 22
7.2.21 Register 0xA119: Boot Status Register 23
7.2.22 Register 0xA11A: Boot Control Clear Register 23
7.2.23 Register 0xA11B: COMe Type Register 23

7.2.24 Register 0xA11C: COMe Current Status Register 23
7.2.25 Register 0xA120: Interrupt0 Port Status Register 23
7.2.26 Register 0xA121: INT0 Source Status Register 23
7.2.27 Register 0xA122: INT0 Source Interrupt Register 24
7.2.28 Register 0xA123: INT0 Source Mask Register 24
7.2.29 Register 0xA124: Interrupt1 Port Status Register 24
7.2.30 Register 0xA125: INT1 Source Status Register 24
7.2.31 Register 0xA126: INT1 Source Interrupt Register 25
7.2.32 Register 0xA127: INT1 Source Mask Register 25
7.2.33 Register 0xA12A: USB_LC_STATE Register 25
7.2.34 Register 0xA12B: EEPROM Write Protect Control Register 25
7.2.35 Register 0xA130: FAN WDT CTRL Register 26
7.2.36 Register 0xA131: FAN1 Front Fan Speed Register 26
7.2.37 Register 0xA132: FAN1 PWM Control Register 26
7.2.38 Register 0xA133: FAN1 LED Control Register 26
7.2.39 Register 0xA135: FAN2 Front Fan Speed Register 26
7.2.40 Register 0xA136: FAN2 PWM Control Register 26
7.2.41 Register 0xA137: FAN2 LED Control Register 27
7.2.42 Register 0xA139: FAN3 Front Fan Speed Register 27
7.2.43 Register 0xA13A: FAN3 PWM Control Register 27
7.2.44 Register 0xA13B: FAN3 LED Control Register 27
7.2.45 Register 0XA140: SI5332_CTRL Register 27
7.2.46 Register 0xA141: PSU Control & Status Register 27
7.2.47 Register 0xA142: PSU LED Software Control Register 28
7.2.48 Register 0xA143: System LED Control Register 28
7.2.49 Register 0xA144: Alarm Status LED Control Register 28
7.2.50 Register 0xA145: Thermal Shutdown Control Register 29
7.2.51 Register 0xA146: Thermal Shutdown Status Register 29
7.2.52 Register 0xA147: PRT_MDSL_TXFLT Register 29
7.2.53 Register 0xA148: PRT_INT_RXLOS Register 30
7.2.54 Register 0xA149: PRT_PRSNT_MODABS Register 31
7.2.55 Register 0xA14A: PRT_LPM_TXDIS Register 31
7.2.56 Register 0XA150: PHY_LOS_Register 32
7.2.57 Register 0xA151: IPROC_GPIO_Register 32
7.2.58 Register 0XA152: SW_ROV_Register 33
7.2.59 Register 0xA153: POWER_EN_STATE – POWER EN STATE Register 33
7.2.60 Register 0xA154: POWER_GOOD_STATE Register 33
7.2.61 Register 0xA161: Watchdog set timer high values Register 33
7.2.62 Register 0xA162: Watchdog set timer middle values Register 33
7.2.63 Register 0xA163: Watchdog set timer low values Register 33
7.2.64 Register 0xA164: Watchdog use timer high values Register 34
7.2.65 Register 0xA165: Watchdog use timer middle values Register 34
7.2.66 Register 0xA166: Watchdog use timer low values Register 34
7.2.67 Register 0xA167: Watchdog function enable Register 34
7.2.68 Register 0xA168: Feeding the dog signal generation Register 34
7.2.69 Register 0xA169: Watchdog timer punch Register 34
7.2.70 Register 0x180: OVERLOAD_CPU_ASIC Register 35
7.2.71 Register 0xA188: FAN Misc Control Register 35
7.2.72 Register 0xA1F0: SF_BACKUP_1 Register 35
7.2.73 Register 0xA1F1: SF_BACKUP_2 Register 35
7.2.74 Register 0xA1F2: SF_BACKUP_3 Register 35
7.2.75 Register 0xA181: Switch power control Register 35
7.2.76 Register 0xA1F3: FW SIGN Register 35

8 References 37

3 Table of Figures

Figure 1: CPLD Functions **9**
Figure 2: Power On Timing **10**
Figure 3: Power Off Timing **10**
Figure 4: I2C Write & Read format **12**
Figure 5: FAN Control **12**
Figure 6: Speed VS PWM Control **13**
Figure 7: TACH waveform **13**
Figure 9: Reset Topology **14**
Figure 10: Interrupt Topology **14**
Figure 11: Interrupt Logic **15**
Figure 12: BIOS Boot Flow **15**

4 Table of Tables

Table 1 – Glossary **2**
Table 2 – CPLD Register Table **17**
Table 3 – CPLD Version Register **19**
Table 4 – Software Scratch Register **20**
Table 5 – MONTH Register **20**
Table 6 – DATA Register **20**
Table 7 – CPLD Bit Source Register **20**
Table 8 – CPU Reset Source Register **20**
Table 9 – Reset Control Register **21**
Table 10 – BCM56277 Reset Control Register **21**
Table 11 – CB_RST_N Mask Register **21**
Table 12 – PHY1 Reset Control Register **21**
Table 13 – PHY2 Reset Control Register **21**
Table 14 – PHY3 Reset Control Register **22**
Table 15 – COMe Power Control Register **22**
Table 16 – COMe Reset Control Register **22**
Table 17 – COMe Status Register **22**
Table 18 – COMe BIOS Disable Control Register **22**
Table 19 – COMe_BIOS_DIS_CTRL Register **23**
Table 20 – COMe Power Button Control Register **23**
Table 21 – RTC_CLEAR_CTRL Register **23**
Table 22 – Power Cycle Control Register **23**
Table 23 – Boot Status Register **23**
Table 24 – Boot Control Clear Register **24**
Table 25 – COMe Type Register **24**
Table 26 – COMe Current Status Register **24**
Table 27 – Interrupt0 Port Status Register **24**
Table 28 – INT0 Source Status Register **24**
Table 29 – INT0 Source Interrupt Register **25**
Table 30 – INT0 Source Mask Register **25**
Table 31 – Interrupt1 Port Status Register **25**
Table 32 – INT1 Source Status Register **25**
Table 33 – INT1 Source Interrupt Register **26**
Table 34 – INT1 Source Mask Register **26**
Table 35 – USB_LC_STATE Register **26**
Table 36 – EEPROM Write Protect Control Registerr **26**
Table 37 – FAN WDT CTRL Register **26**
Table 38 – FAN1 Front Fan Speed Register **27**
Table 39 – FAN1 PWM Control Register **27**
Table 40 – FAN1 LED Control Register **27**
Table 41 – FAN2 Front Fan Speed Register **27**
Table 42 – FAN2 PWM Control Register **27**
Table 43 – FAN2 LED Control Register **27**
Table 44 – FAN3 Front Fan Speed Register **28**
Table 45 – FAN3 PWM Control Register **28**
Table 46 – FAN3 LED Control Register **28**
Table 47 – SI5332_CTRL Register **28**
Table 48 – PSU Control&Status Register **28**
Table 49 – PSU LED Software Control Register **29**
Table 50 – System Control Register **29**

Table 51 – Alarm Status LED Control Register **29**
Table 52 – Thermal Shutdown Control Register **30**
Table 53 – Thermal Shutdown Statu Register **30**
Table 54 **– Port Control Register** **30**
Table 55 **– Port Status Register** **30**
Table 56 **– Port Interrupt Statusl Register** **31**
Table 57 **– Port TxDIS Register** **31**
Table 58 **– PHY LOSl Register** **32**
Table 59 – IPROC GPIO Register **32**
Table 60 – SW ROV Register **32**
Table 61 – POWER EN STATE Register **33**
Table 62 **– POWER GOOD STATEl Register** **33**
Table 63 **– Watchdog set high timer values Register** **33**
Table 64 **– Watchdog set middle timer values Register** **33**
Table 65 **– Watchdog set low timer values Register** **33**
Table 66 **– Watchdog use high timer values Register** **34**
Table 67 **– Watchdog use middle timer values Registerr** **34**
Table 68 **– Watchdog use low timer values Register** **34**
Table 69 **– Watchdog function enable Register** **34**
Table 70 – Feeding the dog signal Register **34**
Table 71 – Watchdog timer punch Register **34**
Table 72 – OVERLOAD_CPU_ASIC Register **35**
Table 73 **– Fan_Misc_contrl Register** **35**
Table 74 **– SF_BACKUP_1 Register** **35**
Table 75 **– SF_BACKUP_2 Register** **35**
Table 76 **– SF_BACKUP_3 Register** **35**
Table 77 **– Switch power control Register** **37**
Table 78 **– FW SIGN Register** **37**

5 Introduction

This document is the design specification for DS1000 Board CPLD.

5.1 Audience

The intended audience of this document is:

- Architects
- System engineers
- Hardware designers
- Software developers
- Functional/In-circuit/system test engineers

5.2 Purpose

The purpose of the document is to convey detailed operation and functionality of the DS1000 Board CPLD.

5.3 Glossary

Table 1 – Glossary

Term / Abbreviation	Definition

6 Functional Description

6.1 Functionality

6.1.1 Feature List

There is only one CPLD in DS1000 Board. The type of CPLD is: LCMXO2-2000HC-4FTG256C. The main functions of CPLD are as follows：

- Power sequence controlling
- LPC accessed by CPU
- I2C bus
- CPU BIOS Select
- Thermal merge
- Reset and Interrupt
- Watchdog
- SFP+ status monitor and controlling
- System status LED control.

The CPU communicates with Switch Board CPLD by I2C interface or LPC interface. The CPLD function shows below.

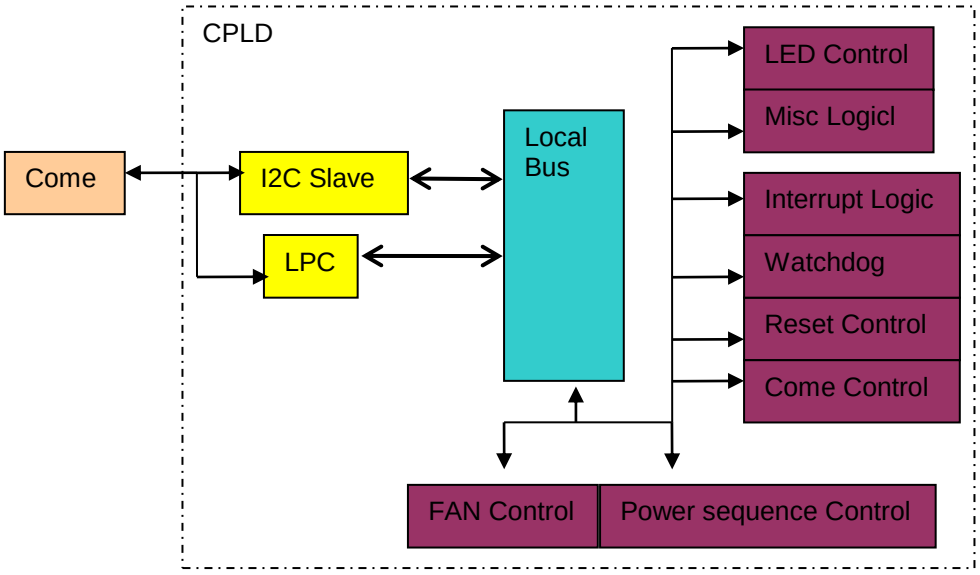


Figure 1: CPLD Functions

6.1.2 Power Control

6.1.2.1 System Power Sequence.

CPLD will control the system power on sequence.
Power on sequence is, after AC cable present in, CPLD power supply rail will auto power on, after CPLD finished initial, CPLD will power on COMe. COMe will enter S5 status after power on, CPLD will auto trig a power button event to COMe and COMe will wake up from S5 to S0. During COMe status change COMe will change signal(SUS_S3_N/SUS_S4_N/SUS_S5_N/ SUS_STAT_N) status to indicate current COMe status. CPLD will use COMe send out SUS_S4_N signal to control Switch Card power enable.

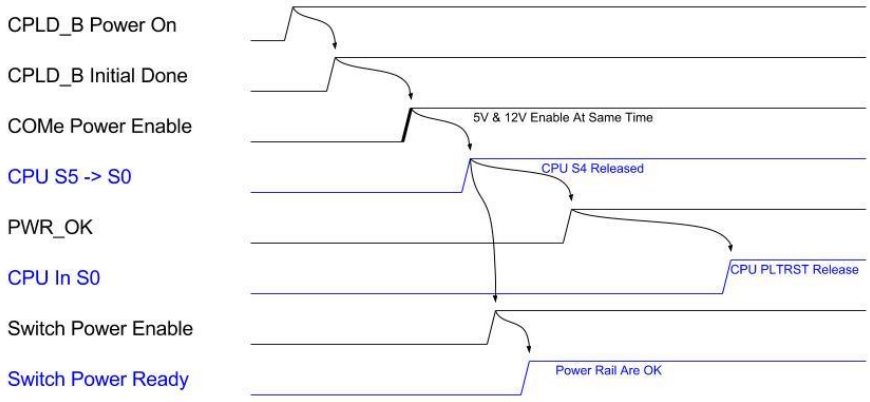


Figure 2: Power On Timing

Power off sequence is, after BMC set the power button over 4S low in CPLD or CPU get a power off CMD from CLI, COMe will start power off sequence, then COMe S4 will goes low, Switch Card will goes low also. Finally COMe will stay in S5 status. And Switch Card in power off status.

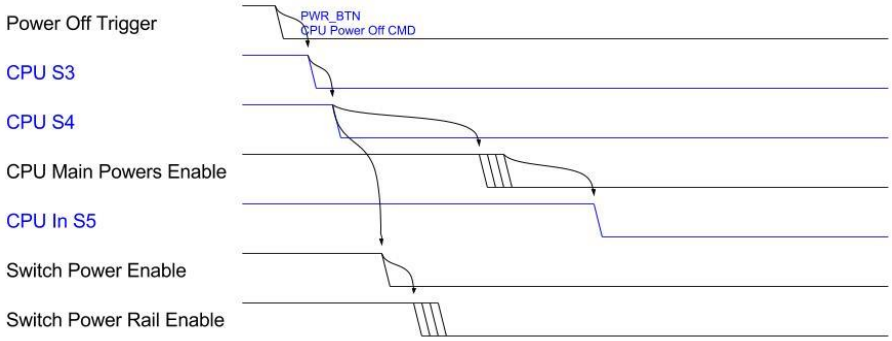


Figure 3: Power Off Timing

6.1.2.2 Switch Power sequence

CPLD will control the switch board the power sequence, The following figure shows the power sequence flow.

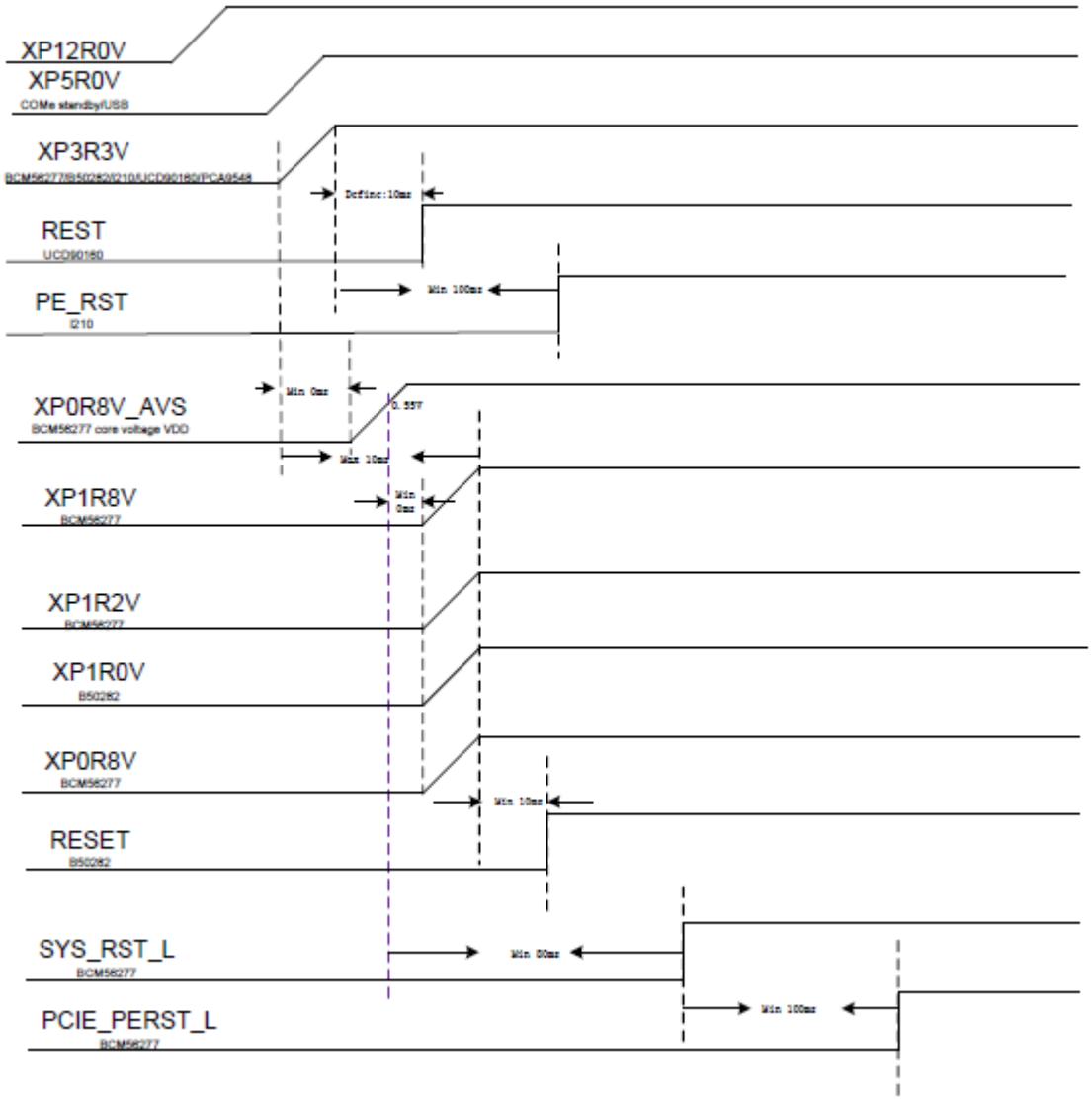


Figure 4: Switch Power sequence

6.1.3 I2C Slave Interface

The CPLD have two I2C slave module (slave address 0x0D) for BMC and CPU to access CPLD registers. The I2C slave module can support 8 bits register address and 8 bits write/read data. The write and read format of I2C are show in figure below.

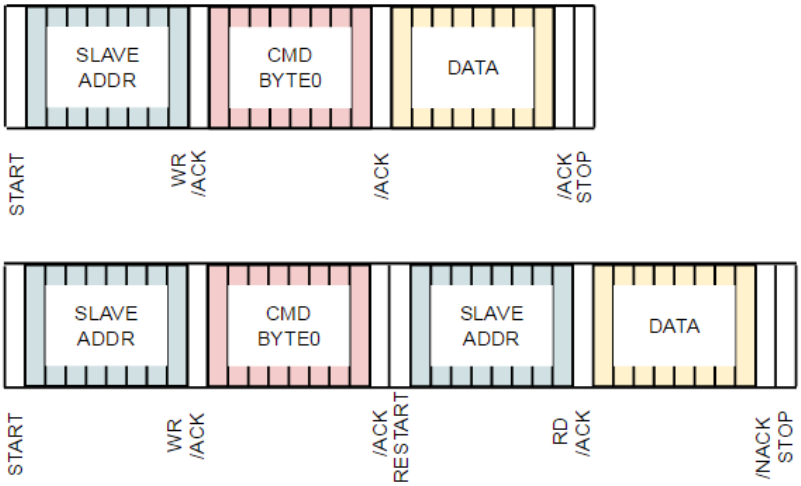


Figure 5 I2C Write & Read format

To execute an I2C write cycle:
1. I2C master send I2C write with 8 bits register address and 8 bits write data;
2. I2C slave module return acknowledge I2C master if received I2C slave address matches with setting;
3. I2C slave module send write data to register.

To execute an I2C read cycle:
1. I2C master send I2C read with 8 bits register address;
2. I2C slave module return acknowledge I2C master if received I2C slave address matches with setting;
3. I2C slave module get read data from register and send back to I2C master;

6.1.4 FAN Control

6.1.4.1 FAN speed control

CPLD control the FAN LED, PWM and check the FAN TACH signals.

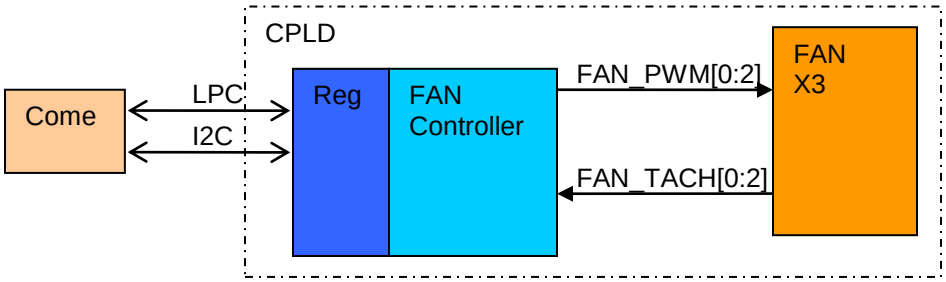


Figure 6: FAN Control

Speed VS PWM control signal is shown below. The preferred operating point for the fan is 26KHz.
The counting period of PWM signal is from 0 to 0xFF. Setting different percentage of 8'hFF can control the speed. For instance, to set 50% duty cycle, 0x7F should be written into PWM control register.

■ Duty Cycle v.s. Speed curve @ Vcc= rated volt.

PWM控制頻率: 26KHz

Duty Cycle(%)	0%	10%	20%	30%	40%	50%	60%	70%	80%	90%	100%
Typ.	0	2800	5700	8600	11400	14300	17200	20000	22900	25700	28600
LIMITS(+)	0	3250	6270	9460	12540	15730	18920	22000	25190	28270	31460
LIMITS(-)	0	2350	5130	7740	10260	12870	15480	18000	20610	23130	25740

Figure 7: Speed VS PWM Control

To get the fan speed, CPLD counter will count clock cycle of TACH signal every 400ms and store the value m in speed register. 400ms = 1/2 *TS * m. To calculate N using formula 60/N = T1 + T2 + T3 +T4=T shown below. The formula can be transformed as 60*1000/N =800/m. Rotate Per Minute (RPM), N = 75* m.

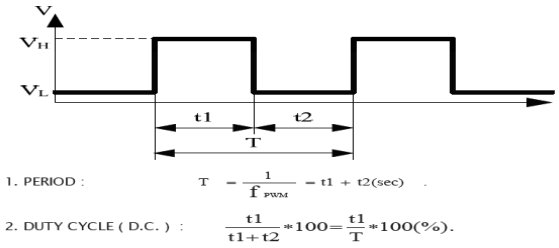


Figure 8: TACH waveform

6.1.4.2 FAN WDT

CPLD shall set FAN speed to 100% if no control from CPU for certain time. The function description as below:
Add FAN_WDT_EN register in CPLD. By default the FAN WDT is disabled. And after FSC start run, FSC set the FAN WDT to enable status.
And in FSC needs write the PWM_CTRL set FAN speed, CPLD will detect the write operation and use the write event to clear the FAN WDT.
When FSC software abnormal hang and didn't write the PWM_CTRL over 300S, CPLD will set the FAN speed to 100%.

6.1.5 Reset Topology

The reset topology is demonstrated below

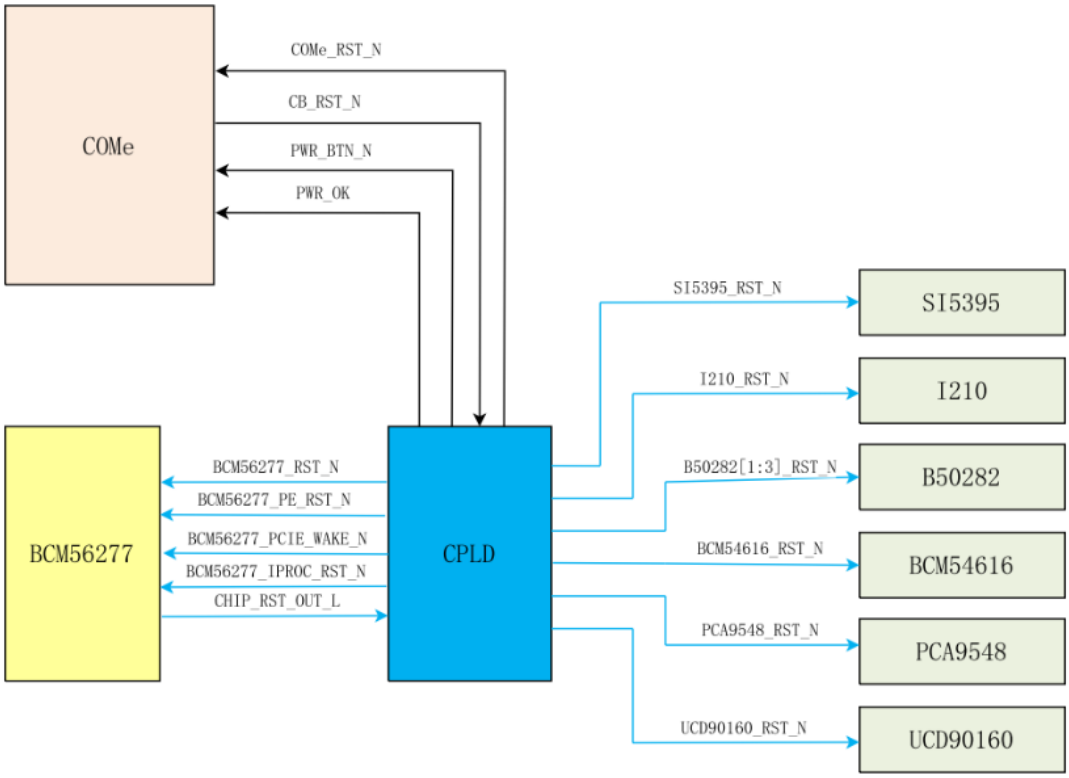


Figure 4: Reset Topology

6.1.6 Interrupts

The interrupt topology is demonstrated below

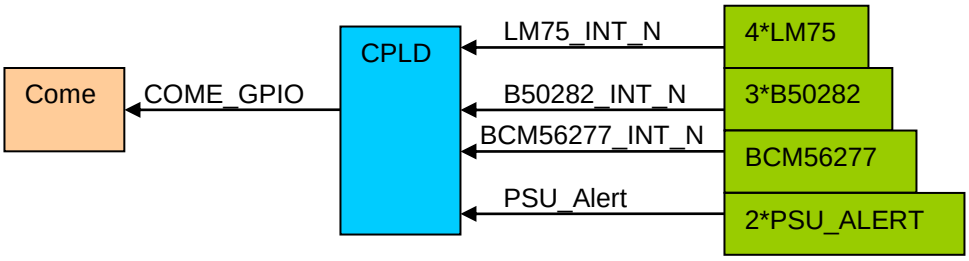


Figure 5: Interrupt Topology

The INT logic details below. Each interrupt has 3 related registers. The Interrupt Status Reg is read only register that indicates the status of interrupt source input. The Interrupt Mask Reg is write/read register used to mask the interrupt source. The Interrupt Flag Reg is read clear register used to indicate the status of interrupt source have changed active.

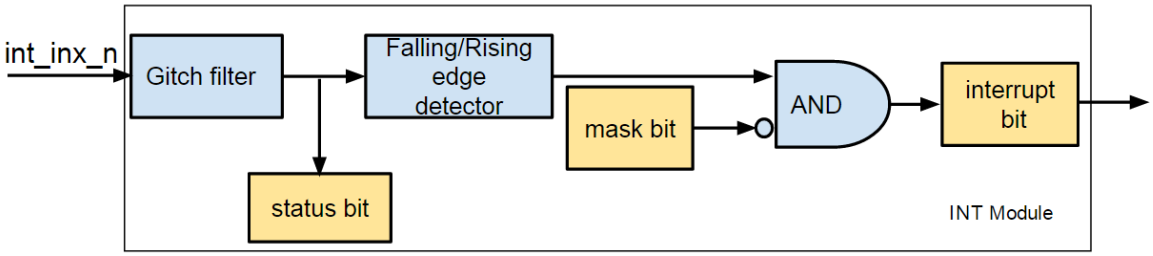


Figure 6: Interrupt Logic

6.1.7 BIOS Boot Control

The system boots from BIOS0 on base board by default. When CPU transfers from S5 to S0, a counter in CPLD begins to monitor the boot time. BIOS needs set the boot ok register in CPLD to stop the counter. If BIOS fails to set boot ok in 130s, CPLD will power off the system and swap to boot from BIOS1 on base board. CPLD provides registers to indicate the boot status.

To update the corrupted BIOS, CPLD provides registers for software to force the control of BIOS selection.

After completing the update, software can set register (0xA164) in CPLD to power cycle CPU (S0->S5->G3->S5->S0).

The following figure shows the BIOS boot flow.

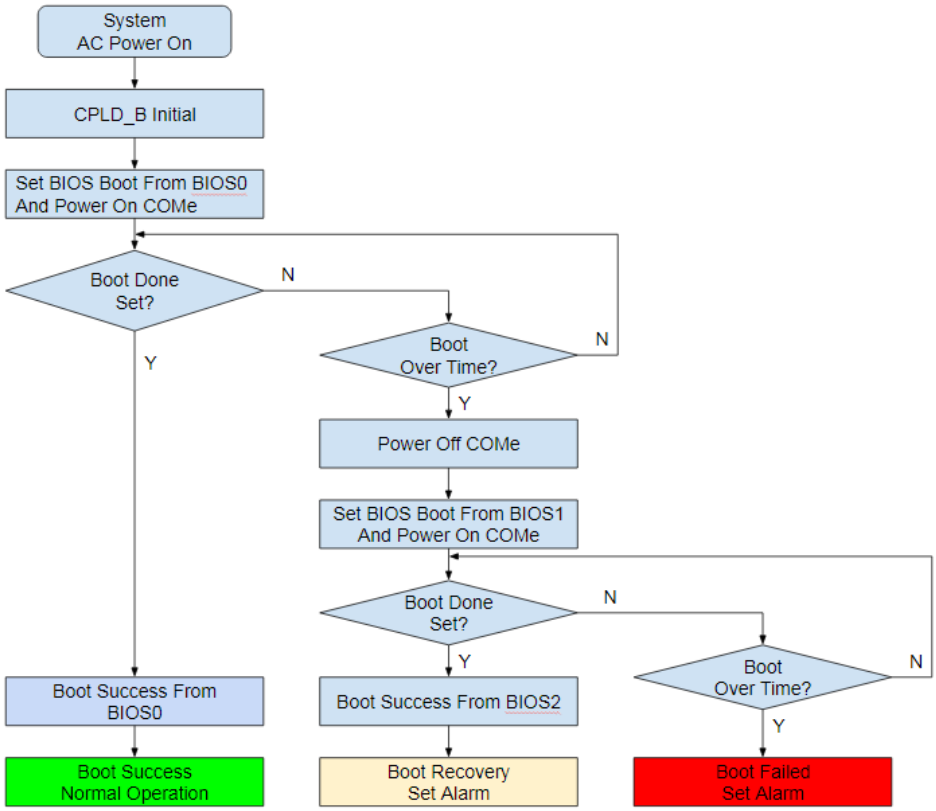


Figure 7: BIOS Boot Flow

6.1.8 Thermal Shutdown Control

CPLD will power off CPU when any sensor LM75 is overheated and set fans to full speed. To enable the function, software needs set the related bit in register.
CPLD provides registers to record the thermal shutdown and indicates which LM75 triggers the event.

6.1.9 LED Control

Base Board CPLD controls the following LEDs:

1. Fan LED. FAN Status LED HW control logic.
a. All FAN Present and status are normal. FAN Status LED Green On.
b. Any one of the FAN is absent, or any of the FAN status is abnormal. Fan Status LED Amber On.
c. All FAN tray are absent, Fan Status LED Off. But usually this condition is not allowed and system will power off if no FAN tray is present.

2. Alarm LED. CPLD Register to control the Alarm Status LED. The Alarm LED support mode include:
a. Off
b. Green LED on (No Alarm)
c. Amber LED on (Critical Alarm)
d. Amber LED 4Hz Blinking (Major Alarm)
e. Amber LED 1Hz Blinking (Minor Alarm)

3. PSU LED. PSU Status LED HW control logic.
a. Both PSU Present and status (PWOK and ALERT_N) are correct. PSU Status LED Green On.
b. One PSU Absent or any one of the PSU status (PWOK or ALERT_N) is incorrect. PSU Status LED Amber On.
c. PSU Status LED Off is not allowed

4. System LED.
1) The System LED support mode include:
a. Off
b. Green LED on
c. Amber LED on
d. Green LED 1Hz Blinking
e. Amber LED 1Hz Blinking
f . Green LED 4Hz Blinking
g. Amber LED 4Hz Blinking
h. Green and Amber LED Alternate1Hz Blinking
i. Green And Amber LED Alternate 4Hz Blinking (Default setting in CPLD)
2) When CPU reset (cold/warm) the LED should return to default mode.
3) For ONIE installed system, after ONIE boot success, ONIE set the LED to Green and Amber LED Alternate1Hz Blinking.
4) For NOS installed system, the System Status LED control by NOS.

7 Software Interface

7.1 Register mapping

The registers are mapped to CPLD:

Table 2 – CPLD Register Table

Register	Description
0xA100	CPLD_B Version Register
0xA101	CPLD_B Software Scratch Register
0xA102	CPLD_B MONTH Register
0xA103	CPLD_B DATA Register
0xA104	CPLD Bit Source Register
0xA105	CPU Reset Source Register
0xA106	Reset Control Register
0xA107	BCM56277 Reset Control Register
0xA108	CB_RST_N Mask Register
0xA109	PHY1 Reset Control Register
0xA10A	PHY2 Reset Control Register
0xA110	PHY3 Reset Control Register
0xA111	COMe Power Control Register
0xA112	COMe Reset Control Register
0xA113	COMe Status Register
0xA114	COMe BIOS Disable Control Register
0xA115	COMe_BIOS_DIS_CTRL Register
0xA116	COMe Power Button Control Registe
0xA117	RTC_CLEAR_CTRL Register
0xA118	Power Cycle Control Register
0xA119	Boot Status Register
0xA11A	Boot Control Clear Register
0xA11B	COMe Type Register
0xA11C	COMe Current Status Register
0xA120	Interrupt0 Port Status Register
0xA121	INT0 Source Status Register
0xA122	INT0 Source Interrupt Register
0xA123	INT0 Source Mask Register
0xA124	Interrupt1 Port Status Register
0xA125	INT1 Source Status Register
0xA126	INT1 Source Interrupt Register
0xA127	INT1 Source Mask Register
0xA12A	USB_LC_STATE Register
0xA12B	EEPROM Write Protect Control Register
0xA130	FAN WDT CTRL Register
0xA131	FAN1 Front Fan Speed Register

0xA132	FAN1 PWM Control Register
0xA133	FAN1 LED Control Register
0xA135	FAN2 Front Fan Speed Register
0xA136	FAN2 PWM Control Register
0xA137	FAN2 LED Control Register
0xA139	FAN3 Front Fan Speed Register
0xA13A	FAN3 PWM Control Register
0xA13B	FAN3 LED Control Register
0Xa140	SI5332_CTRL Register
0xA141	PSU Control & Status Register
0xA142	PSU LED Software Control Register
0xA143	System LED Control Register
0xA144	Alarm Status LED Control Register
0xA145	Thermal Shutdown Control Register
0xA146	Thermal Shutdown Status Register
0xA147	PRT_MDSL_TXFLT Register
0xA148	PRT_INT_RXLOS Register
0xA149	PRT_PRSNT_MODABS Register
0xA14A	PRT_LPMD_TXDIS Register
0xA150	PHY_LOS_Register
0xA151	IPROC_GPIO_Register
0xA152	SW_ROV_Register
0xA153	POWER EN STATE Register
0xA154	POWER_GOOD_STATE Register
0xA161	Watchdog set timer high values Register
0xA162	Watchdog set timer middle values Register
0xA163	Watchdog set timer low values Register
0xA164	Watchdog use timer high values Register
0xA165	Watchdog use timer middle values Register
0xA166	Watchdog use timer low values Register
0xA167	Watchdog function enable Register
0xA168	Feeding the dog signal generation Register
0xA169	Watchdog timer punch Register
0xA180	OVERLOAD_CPU_ASIC Register
0xA188	FAN Misc Control Register
0xA1F0	SF_BACKUP_1 Register
0xA1F1	SF_BACKUP_2 Register
0xA1F2	SF_BACKUP_3 Register
0xA181	Switch power control Register
0xA1F3	FW SIGN Register

7.2 Registers in CPLD_B

7.2.1 Register 0xA100: CPLD_B Version Register

Table 3– CPLD Version Register

Bit #	R/W	Default Value	Description
[7:4]	RO	Designed	CPLD_B major version. The first version is 1.
[3:0]	RO	Designed	CPLD_B minor version. The first version is 0.

7.2.2 Register 0xA101: CPLD_B Software Scratch Register

Table 4– Software Scratch Register

Bit #	R/W	Default Value	Description
[7:0]	R/W	0xDE	Scratchpad for software use. Shall reset to default when got POR reset.

7.2.3 Register 0xA102: CPLD_B MONTH Register

Table 5 – MONTH Register

Bit #	R/W	Default Value	Description
[7:0]	R/W	0x04	CPLD_B create month, The first month is 4.

7.2.4 Register 0xA103: CPLD_B DATA Register

Table 6 – DATA Register

Bit #	R/W	Default Value	Description
[7:0]	R/W	0x23	CPLD_B create data, The first data is 0x23.

7.2.5 Register 0xA104: CPLD Bit Source Register

Table 7– CPLD Bit Source Register

Bit #	R/W	Default Value	Description
[7:0]	RO	0xa0	CPLD bit source: 0xa0:bit from cpld 0xa1:bit from external spi flash

7.2.6 Register 0xA105: CPU Reset Source Register

Table 8 – CPU Reset Source Register

Bit #	R/W	Default Value	Description
[7:0]	RO	0x11	0x00: The last reset is power cycle reset (set register 0xA118) 0x11: The last reset is Power on reset. 0x22: The last reset is soft-set CPU warm reset (set register 0xA112) 0x33: The last reset is soft-set CPU cold reset (set register 0xA116) 0x44: The last reset is CPU warm reset. 0x55: The last reset is CPU cold reset. 0x66: The last reset is CPU GPIO request warm reset.

			0x77: The last reset is watchdog reset. 0x88: cpu overload reboot 0x99: asic overload reboot 0xaa: insufficient fan speed reboot Default: The last reset is Power on reset.

7.2.7 Register 0xA106: Reset Control Register

Table 9 – Reset Control Register

Bit #	R/W	Default Value	Description
[7:5]	RO	0b0	reserved
[4]	R/W	0b1	10GPHY_LED Reset Control 0: Reset 1: Not reset
[3]	R/W	0b1	GPHY_LED Reset Control 0: Reset 1: Not reset
[2]	R/W	0b1	PCA9548_1 Reset Control 0: Reset 1: Not reset
[1]	R/W	0b1	PCA9548_0 Reset Control 0: Reset 1: Not reset
[0]	R/W	0b1	I210 Reset Control 0: Reset 1: Not reset

7.2.8 Register 0xA107: BCM56277 Reset Control Register

Table 10 – BCM56277 Reset Control Register

Bit #	R/W	Default Value	Description
[7:4]	RO	0b0	resevered
[3]	RO	0b1	BCM56277 CHIP_RST_OUT Reset Control 0: Reset 1: Not reset
[2]	R/W	0b1	BCM56277 Reset Control 0: Reset 1: Not reset
[1]	R/W	0b1	BCM56277_PE Reset Control 0: Reset 1: Not reset
[0]	R/W	0b1	BCM56277_IPROC Reset Control 0: Reset 1: Not reset

7.2.9 Register 0xA108: CB_RST_N Mask Register

Table 11 – CB_RST_N Mask Register

Bit #	R/W	Default Value	Description
[7:1]	RO	0x0	Reserved.
[0]	RW	0b0	When this bit set to 1'b1, CB_RST_N is ignored and switch board will not reset during CPU reset. 1: Enable the mask 0: Disable the mask

7.2.10 Register 0xA109: PHY1 Reset Control Register

Table 12 – PHY Reset Control Register

Bit #	R/W	Default Value	Description
[7:1]	RO	0b0	Reserved
[0]	RW	0b1	Control the state of signal B50282_1_RST_N:

			“1” = Normal “0” = Reset

7.2.11 Register 0xA10A: PHY2 Reset Control Register

Table 13 – PHY Reset Control Register

Bit #	R/W	Default Value	Description
[7:1]	RO	0b0	Reserved
[0]	RW	0b1	Control the state of signal B50282_1_RST_N: “1” = Normal “0” = Reset

7.2.12 Register 0xA110: PHY3 Reset Control Register

Table 14 – PHY Reset Control Register

Bit #	R/W	Default Value	Description
[7:1]	RO	0b0	Reserved
[0]	RW	0b1	Control the state of signal B50282_1_RST_N: “1” = Normal “0” = Reset

7.2.13 Register 0xA111: COMe Power Control Register

Table 15 – COMe Power Control Register

Bit #	R/W	Default Value	Description
[7:2]	RW	0x3F	Reserved.
[1]	RW	0b1	PWR_COMe_FORCE Control When this bit set to 0, the CPLD will force the COMe module power off.
[0]	RW	0b1	PWR_COME_EN 0: COMe power is OFF 1: COMe power is ON

7.2.14 Register 0xA112: COMe Reset Control Register

Table 16 – COMe Reset Control Register

Bit #	R/W	Default Value	Description
[7:1]	RO	0x7F	Reserved
[0]	RW	0x1	COMe_RST_N 0: write 0 to trigger COMe reset 1: normal

7.2.15 Register 0xA113: COMe Status Register

Table 17 – COMe Status Register

Bit #	R/W	Default Value	Description
[7:4]	RO	0x0	Reserved.
[3]	RO	0b0	COMe Module SUS_STAT_N Status.
[2]	RO	0b0	COMe Module SUS_S5_N Status.

[1]	RO	0b0	COMe Module SUS_S4_N Status.
[0]	RO	0b0	COMe Module SUS_S3_N Status.

7.2.16 Register 0xA114: COMe BIOS Disable Control Register

Table 18 – COMe BIOS Disable Control Register

Bit #	R/W	Default Value	Description
[7:6]	RO	0x3	Reserved.
[5:4]	RW	0x1	Software force control of BIOS selection 01: Disable. BIOS SPI signal connect to CPU, BIOS selection is controlled by CPLD logic. 00: Enable. BIOS SPI signal connect to CPU, BIOS selection is controlled by software using bit[1:0]
[3:2]	RO	0x0	Reserved
[1:0]	RW	0x1	Control BIOS0 or BIOS1 selection 01: Selection BIOS0 11: Selection BIOS1

Note: after switching bios you need to use the following command “ipmitool power cycle”.

7.2.17 Register 0xA115: COMe_BIOS_DIS_CTRL Register

Table 19 – COMe BIOS DIS Control Register

Bit #	R/W	Default Value	Description
[7:2]	RW	0x3F	Reserved.
[1]	RW	0b0	Control COMe BIOS DIS1
[0]	RW	0b1	Control COMe BIOS DIS0

7.2.18 Register 0xA116: COMe Power Button Control Register

Table 20 – COMe Power Button Control Register

Bit #	R/W	Default Value	Description
[7:1]	RW	0x0	Reserved.
[0]	RW	0b1	Control the net CB_PWR_BTN_N

7.2.19 Register 0xA117: RTC_CLEAR_CTRL Register

Table 21– RTC Clear Control Register

Bit #	R/W	Default Value	Description	Name
[7:1]	RO	0x7F	Reserved	Reserved
[0]	RO	1b0	Control The Status of RTC_CLEAR	RTC_CLEAR_CTRL

7.2.20 Register 0xA118: Power Cycle Control Register

Table 22– Power Cycle Control Register

Bit #	R/W	Default Value	Description
[7:1]	RO	0x0	Reserved.
[0]	R/W	0b1	Enable CPU power cycle. Once enabled, CPLD will power cycle the CPU. The bit will auto set high after CPU power cycle finish. 1: Disable. 0: Enable.

7.2.21 Register 0xA119: Boot Status Register

Table 23 – Boot Status Register

Bit #	R/W	Default Value	Description
[7:2]	RO	0x0	Reserved.
[1]	RO	0b0	0: Indicate CPU boots from BIOS0. 1: Indicate CPU boots from BIOS1.
[0]	R/W	0b0	Used for BIOS to set the boot OK. 0: Indicate CPU boots not ok. 1: Indicate CPU boots ok. Note: The bit can not be write by BMC I2C command

7.2.22 Register 0xA11A: Boot Control Clear Register

Table 24 – Boot Counter Clear Register

Bit #	R/W	Default Value	Description
[7:0]	WO	0x0	Used to clear the boot counter. Write 0xC to this register to reset the boot counter. The counter will then increment from zero again. To prevent from boot overtime (80s) in special case, repeatedly write the register with 0xC

7.2.23 Register 0xA11B: COMe Type Register

Table 25 – COMe Type Register

Bit #	R/W	Default Value	Description
[7:4]	RO	0x0	Reserved.
[2:0]	RO	None	The status of CB_TYPE[2:0]_N

7.2.24 Register 0xA11C: COMe Current Status Register

Table 26 – COMe Status Register

Bit #	R/W	Default Value	Description
[7:0]	RO	0x08	COMe Status

7.2.25 Register 0xA120: Interrupt0 Port Status Register

Table 27 – Interrupt Status Register

Bit #	R/W	Default Value	Description
[7:1]	RO	0x7F	Reserved
[0]	RO	0b1	The Status of CP_GPIO_CPU_SUS0 0: INT 1:not INT

7.2.26 Register 0xA121: INT0 Source Status Register

Table 28 – INT0 Source Status Register

Bit #	R/W	Default Value	Description
[7:6]	RO	0x0	Reserved
[5]	RO	0b1	Status of PSU2_ALERT_N 0: Interrupt 1:not Interrupt
[4]	RO	0b1	Status of PSU1_ALERT_N 0: Interrupt 1:not Interrupt
[3]	RO	0b1	Status of LM75_4_INT_N 0: Interrupt 1:not Interrupt

[2]	RO	0b1	Status of LM75_3_INT_N	0: Interrupt 1:not Interrupt
[1]	RO	0b1	Status of LM75_2_INT_N	0: Interrupt 1:not Interrupt
[0]	RO	0b1	Status of LM75_1_INT_N	0: Interrupt 1:not Interrupt

7.2.27 Register 0xA122: INT0 Source Interrupt Register

Table 29 – INT0 Source Interrupt Register

Bit #	R/W	Default Value	Description
[7:6]	RC	0x0	Reserved
[5]	RC	0b0	Interrupt status of PSU2_ALERT_N 1: Intrrupt 0:not Intrrupt
[4]	RC	0b0	Interrupt status of PSU1_ALERT_N 1: Intrrupt 0:not Intrrupt
[3]	RC	0b0	Interrupt status of LM75_4_INT_N 1: Intrrupt 0:not Intrrupt
[2]	RC	0b0	Interrupt status of LM75_3_INT_N 1: Intrrupt 0:not Intrrupt
[1]	RC	0b0	Interrupt Status of LM75_2_INT_N 1: Intrrupt 0:not Intrrupt
[0]	RC	0b0	Interrupt Status of LM75_1_INT_N 1: Intrrupt 0:not Intrrupt

7.2.28 Register 0xA123: INT0 Source Mask Register

Table 30 – INT0 Source Mask Register

Bit #	R/W	Default Value	Description	
[7:6]	RW	0x3	Reserved	
[5]	RW	0b1	Interrupt mask of PSU2_ALERT_N	0:not mask 1:mask
[4]	RW	0b1	Interrupt mask of PSU1_ALERT_N	0:not mask 1:mask
[3]	RW	0b1	Interrupt mask of LM75_4_INT_N	0:not mask 1:mask
[2]	RW	0b1	Interrupt mask of LM75_3_INT_N	0:not mask 1:mask
[1]	RW	0b1	Interrupt mask of LM75_2_INT_N	0:not mask 1:mask
[0]	RW	0b1	Interrupt mask of LM75_1_INT_N	0:not mask 1:mask

7.2.29 Register 0xA124: Interrupt1 Port Status Register

Table 31 – Interrupt Status Register

Bit #	R/W	Default Value	Description	
[7:1]	RO	0x7F	Reserved	
[0]	RO	0b1	The Status of CP_GPIO_CPU_SUS0	0: INT 1:not INT

7.2.30 Register 0xA125: INT1 Source Status Register

Table 32 – INT1 Source Status Register

Bit #	R/W	Default Value	Description	
[7:4]	RO	0b1	Reserved.	
[3]	RO	0b1	Status of BCM56277_PCIE_INT_N	0: Interrupt 1:not Interrupt
[2]	RO	0b1	Status of B50282_3_INT_N	0: Interrupt 1:not Interrupt
[1]	RO	0b1	Status of B50282_2_INT_N	0: Interrupt 1:not Interrupt

[0]	RO	0b1	Status of B50282_1_INT_N	0: Interrupt 1:not Interrupt

7.2.31 Register 0xA126: INT1 Source Interrupt Register

Table 33 – INT1 Source Interrupt Register

Bit #	R/W	Default Value	Description
[7:4]	RC	0b0	Reserved.
[3]	RC	0b0	Interrupt status of BCM56277_PCIE_INT_N 1: Intrrupt 0:not Intrrupt
[2]	RC	0b0	Interrupt status of B50282_3_INT_N 1: Intrrupt 0:not Intrrupt
[1]	RC	0b0	Interrupt status of B50282_2_INT_N 1: Intrrupt 0:not Intrrupt
[0]	RC	0b0	Interrupt status of B50282_1_INT_N 1: Intrrupt 0:not Intrrupt

7.2.32 Register 0xA127: INT1 Source Mask Register

Table 34 – INT1 Source Mask Register

Bit #	R/W	Default Value	Description	
[7:4]	RW	0xf	Reserved.	
[3]	RW	0b1	Interrupt mask of BCM56277_PCIE_INT_N	0:not mask 1:mask
[2]	RW	0b1	Interrupt mask of B50282_3_INT_N	0:not mask 1:mask
[1]	RW	0b1	Interrupt mask of B50282_2_INT_N	0:not mask 1:mask
[0]	RW	0b1	Interrupt mask of B50282_1_INT_N	0:not mask 1:mask

7.2.33 Register 0xA12A: USB_LC_STATE Register

Table 35 – USB_LC_STATE Register

Bit #	R/W	Default Value	Description
[7:2]	RO	0x3F	Reserved.
[1]	RW	0b1	USB_EN2 0: USB EN is OFF 1: USB EN is ON
[0]	RW	0b1	USB_EN1 0: USB EN is OFF 1: USB EN is ON

7.2.34 Register 0xA12B: EEPROM Write Protect Control Register

Table 36 – EEPROM Write Protect Control Register

Bit #	R/W	Default Value	Description
[7:4]	RO	0x0	Reserved
[3]	RW	0b0	Control The Status of BID_EEPROM_WP.
[2]	RW	0b0	Control the status of TLV_EEPROM_WP
[1]	RW	0b1	Control The Status of BIOS_SPI_WP1_N.
[0]	RW	0b1	Control The Status of BIOS_SPI_WP0_N.

7.2.35 Register 0xA130: FAN WDT CTRL Register

Table 37 – FAN WDT Enable Register

Bit #	R/W	Default Value	Description
[7:5]	RO	0x0	Reserved
[4]	RO	0b1	over_time_flag, When time is exceed 300s, this reg will be set 1. 0: Not exceed 300s 1:exceed 300s
[1:3]	RO	0x0	Reserved
[0]	RW	0b1	Enable FAN WDT function 1: FAN WDT enable 0: FAN WDT disable

7.2.36 Register 0xA131: FAN1 Front Fan Speed Register

Table 38 – FAN1 Front Fan Register

Bit #	R/W	Default Value	Description
[7:0]	RO	0xFF	The actual speed(RPM) of the fan and this register value 'm' conversion is as follow: RPM = 150*m

7.2.37 Register 0xA132: FAN1 PWM Control Register

Table 39 – FAN1 PWM Control Register

Bit #	R/W	Default Value	Description
[7:0]	RW	0xFF	FAN PWM Control, Maximum fan speed when it is set to 0xFF.

7.2.38 Register 0xA133: FAN1 LED Control Register

Table 40 – FAN1 LED Control Register

Bit #	R/W	Default Value	Description
[7:2]	RO	0x0	Reserved
[1]	RW	0b0	FAN1 Green LED Control 0:On 1:Off
[0]	RW	0b1	FAN1 amber LED Control 0:On 1:Off

7.2.39 Register 0xA135: FAN2 Front Fan Speed Register

Table 41 – FAN2 Front Fan Register

Bit #	R/W	Default Value	Description
[7:0]	RO	0xFF	The actual speed(RPM) of the fan and this register value 'm' conversion is as follow: RPM = 150*m

7.2.40 Register 0xA136: FAN2 PWM Control Register

Table 42 – FAN2 PWM Control Register

Bit #	R/W	Default Value	Description
[7:0]	RW	0xFF	FAN PWM Control, Maximum fan speed when it is set to 0xFF.

7.2.41 Register 0xA137: FAN2 LED Control Register

Table 43 – FAN2 LED Control Register

Bit #	R/W	Default Value	Description
[7:2]	RO	0x0	Reserved
[1]	RW	0b0	FAN2 Green LED Control 0:On 1:Off
[0]	RW	0b1	FAN2 amber LED Control 0:On 1:Off

7.2.42 Register 0xA139: FAN3 Front Fan Speed Register

Table 44 – FAN3 Front Fan Register

Bit #	R/W	Default Value	Description
[7:0]	RO	0xFF	The actual speed(RPM) of the fan and this register value 'm' conversion is as follow: RPM = 150*m

7.2.43 Register 0xA13A: FAN3 PWM Control Register

Table 45 – FAN3 PWM Control Register

Bit #	R/W	Default Value	Description
[7:0]	RW	0xFF	FAN PWM Control, Maximum fan speed when it is set to 0xFF.

7.2.44 Register 0xA13B: FAN3 LED Control Register

Table 46 – FAN3 LED Control Register

Bit #	R/W	Default Value	Description
[7:2]	RO	0x0	Reserved
[1]	RW	0b0	FAN3 Green LED Control 0:On 1:Off
[0]	RW	0b1	FAN3 amber LED Control 0:On 1:Off

7.2.45 Register 0XA140: SI5332_CTRL Register

Table 47-- SI5332_CTRL Register

Bit #	R/W	Default Value	Description
[7:6]	RO	0x0	Reserved
[0]	RW	0b0	SI5332_OE_N 0:enable 1:not enable

7.2.46 Register 0xA141: PSU Control & Status Register

Table 48 – PSU Control&Status Register

Bit #	R/W	Default Value	Description
[7]	RW	0b1	PSU2 alert status. 0: Alert 1: Not alert
[6]	RW	0b1	PSU1 alert status. 0: Alert 1: Not alert

[5]	RW	0b1	PSU2 present status. 0: Present 1: Absent
[4]	RW	0b1	PSU1 present status. 0: Present 1: Absent
[3]	RW	0b1	PSU2 power OK status 0: Not OK 1: OK
[2]	RW	0b1	PSU1 power OK status 0: Not OK 1: OK
[1]	RW	0b0	PSU2 enable control. 0: On 1: Off
[0]	RW	0b0	PSU1 enable control. 0: On 1: Off

7.2.47 Register 0xA142: PSU LED Software Control Register

Table 49 – PSU LED Software Control Register

Bit #	R/W	Default Value	Description
[7:6]	RO	2b0	Reserved
[5]	RW	0x0	Not used/Reserved
[4]	RW	0x1	0b1: PSU led controlled by hardware Use one PSU, Amber led on Use two PSU, Green led on 0b0: PSU led controlled by software bit [1:0]
[3:2]	RO	None	Reserved
[1]	RW	0b1	0b0: Turn off green led 0b1: Turn on green led
[0]	RW	0b0	0b0: Turn off amber led 0b1: Turn on amber led

7.2.48 Register 0xA143: System LED Control Register

Table 50 – System Control Register

Bit #	R/W	Default Value	Description
[7:6]	RO	0x3	Reserved.
[5:4]	RW	0b00	System LED selection control. Set bits [5:4] to select which LED is used and set bits [1:0] to control the selected LED mode. When both LEDs are used (bits[5:4] = 2'b00), only blink mode are supported. 00:Both green LED & yellow LED are used. When System Status LED control set to blink. The green LED & yellow LED will alternate blinking. 10:Only green LED used. 01:Only yellow LED used. 11:LED are off.
[3]	RO	0b1	Reserved
[2]	RO	0b1	Reserved
[1:0]	RW	0b10	System Status LED Control. 11: Off; 10: 4Hz blink; 01: 1Hz blink; 00: on.

7.2.49 Register 0xA144: Alarm Status LED Control Register

Table 51 – Alarm Status LED Control Register

Bit #	R/W	Default Value	Description
[7:6]	RO	0x3	Reserved.
[5:4]	RW	0b00	Select LED light color 10:Yellow LED used. 01:Green LED used. Other:LED are off.
[3]	RO	0b1	Reserved
[2]	RO	0b1	Reserved
[1:0]	RW	0b00	Alarm Status LED Blink Control. 10: 4Hz blink; 01: 1Hz blink; Other: no blink.

7.2.50 Register 0xA145: Thermal Shutdown Control Register

Table 52 – Thermal Shutdown Control Register

Bit #	R/W	Default Value	Description
[7:1]	RO	0x0	Reserved.
[0]	R/W	0b0	Enable the thermal shutdown. Once enabled, CPLD will power down the CPU when received alarm from LM75. 0: Disable. 1: Enable.

7.2.51 Register 0xA146: Thermal Shutdown Status Register

Table 53 – Thermal Shutdown Status Register

Bit #	R/W	Default Value	Description
[7]	RO	0b0	Reserved.
[6]	RO	0b0	When thermal shutdown occurs, this bit will set to 1'b1 to indicate the event. Refer to bit[2:0] to check LM75 status.
[5:4]	RO	0b0	Reserved
[3]	RO	0b1	Indicate the thermal sensor status. 0: LM75_4 on base board is over temperature 1: LM75_4 is in normal condition
[2]	RO	0b1	Indicate the thermal sensor status. 0: LM75_3 on base board is over temperature 1: LM75_3 is in normal condition
[1]	RO	0b1	Indicate the thermal sensor status. 0: LM75_2 on base board is over temperature 1: LM75_2 is in normal condition
[0]	RO	0b1	Indicate the thermal sensor status. 0: LM75_1 on base board is over temperature 1: LM75_1 is in normal condition

7.2.52 Register 0xA147: PRT_MDSL_TXFLT Register

Table 54 – Port Control Register

Bit #	R/W	Default Value	Description
[7]	RO	0b0	Indicate the SFP+_8_TX_FAULT status. "0" = not detect a fault condition related "1" = detect a fault condition related

[6]	RO	0b0	Indicate the SFP+_7_TX_FAULT status. “0” = not detect a fault condition related “1” = detect a fault condition related
[5]	RO	0b0	Indicate the SFP+_6_TX_FAULT status. “0” = not detect a fault condition related “1” = detect a fault condition related
[4]	RO	0b0	Indicate the SFP+_5_TX_FAULT status. “0” = not detect a fault condition related “1” = detect a fault condition related
[3]	RO	0b0	Indicate the SFP+_4_TX_FAULT status. “0” = Optical module transmitter is turn ON “1” = Optical module transmitter is turn OFF
[2]	RO	0b0	Indicate the SFP+_3_TX_FAULT status. “0” = not detect a fault condition related “1” = detect a fault condition related
[1]	RO	0b0	Indicate the SFP+_2_TX_FAULT status. “0” = not detect a fault condition related “1” = detect a fault condition related
[0]	RO	0b0	Indicate the SFP+_1_TX_FAULT status. “0” = not detect a fault condition related “1” = detect a fault condition related

7.2.53 Register 0xA148: PRT_INT_RXLOS Register

Table 55 – Port Status Register

Bit #	R/W	Default Value	Description
[7]	RO	0b0	Indicate SFP+_8_RXLOS status: “0” = No loss of signal. “1” = Loss of signal.
[6]	RO	0b0	Indicate SFP+_7_RXLOS status: “0” = No loss of signal. “1” = Loss of signal.
[5]	RO	0b0	Indicate SFP+_6_RXLOS status: “0” = No loss of signal. “1” = Loss of signal.
4]	RO	0b0	Indicate SFP+_5_RXLOS status: “0” = No loss of signal. “1” = Loss of signal.
[3]	RO	0b0	Indicate SFP+_4_RXLOS status: “0” = No loss of signal. “1” = Loss of signal.
[2]	RO	0b0	Indicate SFP+_3_RXLOS status: “0” = No loss of signal. “1” = Loss of signal.
[1]	RO	0b0	Indicate SFP+_2_RXLOS status: “0” = No loss of signal. “1” = Loss of signal.
[0]	RO	0b0	RXLOS/INT_N. Applicable to SFP type modules Indicate the Optical module receiver has asserted Loss of Signal or not The bit definition is given below

			For SFP+_1_RXLOS status: “0” = No loss of signal. “1” = Loss of signal.

7.2.54 Register 0xA149: PRT_PRSNT_MODABS Register

Note: The interrupt status bit is valid when its related mask bit is set disabled.

Table 56 – Port Interrupt Status Register

Bit #	R/W	Default Value	Description
[7]	RO	0b1	Indicate SFP+_8_MOD_ABS signal: “0” = present SFP “1” = Not present SFP
[6]	RO	0b1	Indicate SFP+_7_MOD_ABS signal: “0” = present SFP “1” = Not present SFP
[5]	RO	0b1	Indicate SFP+_6_MOD_ABS signal: “0” = present SFP “1” = Not present SFP
4]	RO	0b1	Indicate SFP+_5_MOD_ABS signal: “0” = present SFP “1” = Not present SFP
[3]	RO	0b1	Indicate SFP+_4_MOD_ABS signal: “0” = present SFP “1” = Not present SFP
[2]	RO	0b1	Indicate SFP+_3_MOD_ABS signal: “0” = present SFP “1” = Not present SFP
[1]	RO	0b1	Indicate SFP+_2_MOD_ABS signal: “0” = present SFP “1” = Not present SFP
[0]	RO	0b1	Indicate SFP+_1_MOD_ABS signal: “0” = present SFP “1” = Not present SFP

7.2.55 Register 0xA14A: PRT_LPM_TXDIS Register

Table 57 – Port TxDIS Register

Bit #	R/W	Default Value	Description
[7]	RW	0b0	Indicate SFP+_8_TX_DISABLE status. “0” = Optical module transmitter is turn ON/ The module is not in Low power mode. “1” = Optical module transmitter is turn OFF/ The module is in Low power mode.
[6]	RW	0b0	Indicate SFP+_7_TX_DISABLE status. “0” = Optical module transmitter is turn ON/ The module is not in Low power mode. “1” = Optical module transmitter is turn OFF/ The module is in Low power mode.
[5]	RW	0b0	Indicate SFP+_6_TX_DISABLE status. “0” = Optical module transmitter is turn ON/ The module is not in Low power mode.

			“1” = Optical module transmitter is turn OFF/ The module is in Low power mode.
4]	RW	0b0	Indicate SFP+_5_TX_DISABLE status. “0” = Optical module transmitter is turn ON/ The module is not in Low power mode. “1” = Optical module transmitter is turn OFF/ The module is in Low power mode.
[3]	RW	0b0	Indicate SFP+_4_TX_DISABLE status. “0” = Optical module transmitter is turn ON/ The module is not in Low power mode. “1” = Optical module transmitter is turn OFF/ The module is in Low power mode.
[2]	RW	0b0	Indicate SFP+_3_TX_DISABLE status. “0” = Optical module transmitter is turn ON/ The module is not in Low power mode. “1” = Optical module transmitter is turn OFF/ The module is in Low power mode.
[1]	RW	0b0	Indicate SFP+_2_TX_DISABLE status. “0” = Optical module transmitter is turn ON/ The module is not in Low power mode. “1” = Optical module transmitter is turn OFF/ The module is in Low power mode.
[0]	RW	0b0	TX_DIS/ LPMOD. Applicable to SFP type modules TX_DIS : Optical module transmitter output is turn off or not LPMOD : Enables the Low power mode of the optical module Indicate SFP+_1_TX_DISABLE status. “0” = Optical module transmitter is turn ON/ The module is not in Low power mode. “1” = Optical module transmitter is turn OFF/ The module is in Low power mode.

7.2.56 Register 0XA150: PHY_LOS_Register

Table 58-- PHY_LOS_Register

Bit #	R/W	Default Value	Description
[7:5]	RO	0x0	Reserved.
[4]	RO	0b0	PHY_LOS4
[3]	RO	0b0	PHY_LOS3
[2]	RO	0b0	PHY_LOS2
[1]	RO	0b0	PHY_LOS1
[0]	RO	0b0	PHY_LOS0

7.2.57 Register 0xA151: IPROC_GPIO_Register

Table 59-- IPROC_GPIO_Register

Bit #	R/W	Default Value	Description
[7:4]	RO	0x0	Reserved.
[3]	RO	0b0	IPROC_GPIO3
[2]	RO	0b0	IPROC_GPIO2
[1]	RO	0b0	IPROC_GPIO1
[0]	RO	0b0	IPROC_GPIO0

7.2.58 Register 0XA152: SW_ROV_Register

Table 60-- SW_ROV_Register

Bit #	R/W	Default Value	Description	Name
[7:4]	RO	0x0	Reserved.	Reserved
[3]	RO	0x0	0001：0.800v	AVS3
[2]	RO	0x0	0010：0.825v	AVS2
[1]	RO	0x0	0100：0.850v	AVS1
[0]	RO	0x0	1000：0.875v	AVS0

7.2.59 Register 0xA153: POWER_EN_STATE – POWER EN STATE Register

Table 61 – POWER EN STATE Register

Bit #	R/W	Default Value	Description	Name
[7]	RO	1b0	Resevered	resevered
[6]	RO	1b1	POWER EN	PWR8_XP3R3V_MDIO_EN
[5]	RO	1b1	POWER EN	PWR2_XP1R8V_EN
[4]	RO	1b1	POWER EN	PWR3_XP0R8V_EN
[3]	RO	1b1	POWER EN	PWR7_XP1R2V_EN
[2]	RO	1b1	POWER EN	PWR6_XP1R0V_EN
[1]	RO	1b1	POWER EN	PWR4_XP0R8V_AVS_EN
[0]	RO	1b1	POWER EN	PWR5_XP5R0V_EN

7.2.60 Register 0xA154: POWER_GOOD_STATE Register

Table 62 – POWER GOOD STATE Register

Bit #	R/W	Default Value	Description	Name
[7]	RO	1b1	POWER GOOD	CB_PWR8_3R3V_MDIO_PG
[6]	RO	1b1	POWER GOOD	CB_PWR2_1R8V_PG
[5]	RO	1b1	POWER GOOD	CB_PWR3_0R8V_PG
[4]	RO	1b1	POWER GOOD	CB_PWR7_1R2V_PG
[3]	RO	1b1	POWER GOOD	CB_PWR6_1R0V_PG
[2]	RO	1b1	POWER GOOD	CB_PWR4_0R8V_AVS_PG
[1]	RO	1b1	POWER GOOD	CB_PWR1_3R3V_PG
[0]	RO	1b1	POWER GOOD	CB_PWR5_5R0V_PG

7.2.61 Register 0xA161: Watchdog set timer high values Register

Table 63– Watchdog set high timer values Register

Bit #	R/W	Default Value	Description
[7:0]	R/W	0x00	watchdog set time high values**,**time scale is 1ms

7.2.62 Register 0xA162: Watchdog set timer middle values Register

Table 64– Watchdog set middle timer values Register

Bit #	R/W	Default Value	Description
[7:0]	R/W	0x75	watchdog set time middle values**,**time scale is 1ms

7.2.63 Register 0xA163: Watchdog set timer low values Register

Table 65– Watchdog set low timer values Register

Bit #	R/W	Default Value	Description
[7:0]	R/W	0x30	watchdog set time low values**,**time scale is 1ms

7.2.64 Register 0xA164: Watchdog use timer high values Register

Table 66– Watchdog use high timer values Register

Bit #	R/W	Default Value	Description
[7:0]	RO	0x00	watchdog use time high values**,**time scale is 1ms

7.2.65 Register 0xA165: Watchdog use timer middle values Register

Table 67– Watchdog use middle timer values Register

Bit #	R/W	Default Value	Description
[7:0]	RO	0x75	watchdog use time middle values**,**time scale is 1ms

7.2.66 Register 0xA166: Watchdog use timer low values Register

Table 68– Watchdog use low timer values Register

Bit #	R/W	Default Value	Description
[7:0]	RO	0x30	watchdog use time low values**,**time scale is 1ms

7.2.67 Register 0xA167: Watchdog function enable Register

Table 69 – Watchdog function enable Register

Bit #	R/W	Default Value	Description
[7:1]	RO	0x0	Reserved.
[0]	R/W	0b0	Watchdog function enable bit '1' = watch dog counter working '0' = disable watch dog function

7.2.68 Register 0xA168: Feeding the dog signal generation Register

Table 70– Feeding the dog signal Register

Bit #	R/W	Default Value	Description
[7:1]	RO	0x0	Reserved.
[0]	R/W	0b0	Feeding the dog signal generation '1' = Start feeding signal '0' = End feeding signal

7.2.69 Register 0xA169: Watchdog timer punch Register

Table 71– Watchdog timer punch Register

Bit #	R/W	Default Value	Description
[7:1]	RO	0x0	Reserved.
[0]	R/W	0b1	Watchdog timer punch '0' = when set to 0 by SW, the timer is restarted if WD_EN is set. This bit will be set back to 1 by CPLD '1' = set to 1 has no effect on timer function.

7.2.70 Register 0x180: OVERLOAD_CPU_ASIC Register

Table 72 – OVERLOAD_CPU_ASIC Register

Bit #	R/W	Default Value	Description
[7:0]	RW	0x0	a1 : REBOOT_CAUSE_THERMAL_OVERLOAD_CPU a2 : REBOOT_CAUSE_THERMAL_OVERLOAD_ASIC a3 : REBOOT_CAUSE_insufficient_FAN_SPEED

7.2.71 Register 0xA188: FAN Misc Control Register

Table 73 – Fan_Misc_control Register

Bit #	R/W	Default Value	Description
[7:3]	none	0	Reserved.
[2]	RW	0	FAN3 Direction 0: F2B FAN 1: B2F FAN
[1]	RW	0	FAN2 Direction 0: F2B FAN 1: B2F FAN
[0]	RW	0	FAN1 Direction 0: F2B FAN 1: B2F FAN

7.2.72 Register 0xA1F0: SF_BACKUP_1 Register

Table 74 – SF_BACKUP_1 Register

Bit #	R/W	Default Value	Description
[7:0]	R/W	0x0	Reserved.

7.2.73 Register 0xA1F1: SF_BACKUP_2 Register

Table 75 – SF_BACKUP_2 Register

Bit #	R/W	Default Value	Description
[7:0]	R/W	0x0	Reserved.

7.2.74 Register 0xA1F2: SF_BACKUP_3 Register

Table 76 – SF_BACKUP_3 Register

Bit #	R/W	Default Value	Description
[7:0]	R/W	0x0	Reserved.

7.2.75 Register 0xA181: Switch power control Register

Table 77 – Switch power control Register

Bit #	R/W	Default Value	Description
[7:2]	RO	0x0	Reserved.
[1:0]	RW	0x01	0x01:power on 0x00:power off

7.2.76 Register 0xA1F3: FW SIGN Register

Table 78 – FW sign Register

Bit #	R/W	Default Value	Description
[7:0]	RO	None	0xaa: Offline FW sign 0xbb: Online FW sign

8 References

Rxxxx-Mxxxx-01_R0.1_Questone-2 HW_Design_Specification.doc

END OF DOCUMENT